

**REMARKS**

Claims 16, 18-20, and 22-26 remain for reconsideration. Claims 1-15, 17 and 21 have been cancelled without prejudice or disclaimer.

The objection to the informal drawings is noted. Formal drawings will be prepared and submitted at such time as the claims are allowed.

All remaining claims stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,644,700 to Dickson et al. (Dickson). This rejection is respectfully traversed based on the following discussion taken with the claim amendments.

Briefly, embodiments of the present invention provide a controller mode negotiation protocol. Each system management controller in the system is adapted to perform the negotiation protocol. The negotiation protocol may be performed for events such as system initiation or when a single system management controller performs a reset. For example, when a system is powered on, each system management controller in the system may send a controller mode request to other system management controllers according to the negotiation protocol, and may transition to an initial mode based upon a response to the controller mode request.

As shown in Figure 1, system 100 contains four modules 110, 120,

130, and 140 which may be, for example, circuit boards that are inserted into slots of a system chassis. Each of modules 110, 120, 130, and 140 may be a power supply, fan tray, CPU Board, or any other type of component. The controllers in system 100 may each be coupled through an input/output port to a system management bus 150. As explained on page 5, lines 1-10 the bus 150 may be an Intelligent Platform Management Bus (IPMB) which conforms to the Intelligent Platform Management Bus Communications Protocol Specification. A system management controller may communicate with other system components using various types of message formats such as that defined in the Intelligent Platform Management Interface Specification (Intel Corp. et al., v1.5, rev. 1, February. 21, 2001).

In contrast, the controllers of Dickerson, do not teach or suggest the use of an Intelligent Platform Management Bus (IPMB) to communicate status between the controllers 18 and 19, but rather use an *interconnect cable 23* directly connecting each of the controllers (column 5, line 14).

In addressing Applicant's previous arguments, the Examiner continues to assert that Dickson teaches IPMB. The Examiner asserts that this bus is taught by Figure 1, reference numeral 20. However, that does not appear to be the case. Figure 1, reference numeral 20 shows a SBS (Status Bus Slave) bus, not an IPMB as claimed.

Dickson is assigned on its face to Unisys Corporation. As explained on column 2, beginning at line 22, the SBS bus is believed to be part of

*"the Unisys USP2010 Subsystem, and in the disclosed embodiment is connected to a host computer 14 by means of a bus 15. The SDM 10 includes a plurality of input/output devices, which in the illustrated embodiment comprise disk drives 16A-16F, that are coupled to the SCSI channel 12 for transmission of data to and from the host computer 12 via the port 13. The drives 16A-16F are controlled by a Status Bus Slave ("SBS") apparatus 17 over a set of control lines 24, which is also referred to herein as the backplane.*

*The SBS 17 receives instruction data and control signals from a first Status Bus Master Controller ("SBMC") 18 or a secondary or backup SBMC 19 over a bus 20, which may be coupled to a plurality of SDM'S similar to the SDM 10. Only one of the SBMC's 18 or 19 may be in control of the status bus 20 at any given time. The non-controlling SBMC acts as a Status Bus Slave, receiving instruction data and control signals from the active SBMC over the SBS bus 20 and by an interconnect cable 23".*

Thus, the SBS bus taught by Dickson does not appear to be analogous to the IPMI bus as claimed. In brief, IPMI defines common interfaces to the "intelligent" hardware that is used to monitor server physical health characteristics, such as temperature, voltage, fans, power supplies and chassis. These monitoring abilities provide information that enables system management, recovery and asset tracking, which help drive down the total cost of ownership (TCO) for server users. The specifications interoperability guidelines will enable server OEMs to quickly bring new server hardware with

these advanced capabilities to market efficiently and cost effectively.

Independent Claim 16 recites "wherein the mode requests and responses are sent as messages that comply with the Intelligent Platform Management Interface" (emphasis added).

MPEP § 2131 mandates that "TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT IN THE CLAIM".

Furthermore, the MPEP, citing Richardson v. Suzuki Motor Co., 9 USPQ2d 1051, 1053 (Fed. Cir. 1987), states "[t]he identical invention must be shown in as complete detail as is contained in the... claim" (emphasis added).

Dickson does not teach using an Intelligent Platform Management Bus to communicate between the modules. In contrast, it teaches using a separate interconnect cable which would involve separate cabling between each of the control modules.

It is therefore respectfully submitted that the rejections to the claims are improper under Section 102 as Dickson cannot anticipate the rejected claims since they do not "teach the identical invention". Nor, can Dickson make a case of *prima facie* obviousness under Section 103 since all of the claimed features are not shown or reasonably suggested. Based on the above discussion with reference to the MPEP guidelines, it is respectfully requested that the rejections based on 35 U.S.C. § 102 be withdrawn.

This being the only rejection to the claims it is respectfully requested that these claims be allowed.

In view of the foregoing, it requested that the application be reconsidered, that claims 16, 18-20, and 22-26 be allowed and that the application be passed to issue. Please charge any shortages and credit any overcharges to Intel's Deposit Account number 50-0221.

Respectfully submitted,


/Kevin A. Reif/  
Kevin A. Reif  
Reg. No. 36,381

INTEL  
LF1-102  
4050 Lafayette Center Drive  
Chantilly, Virginia 20151  
(703) 633-6834

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:  
**Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450**

On: December 1, 2005

Signature:

  
Katherine Jennings